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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,532	09/24/2004	Bhupendra SHARMA	TI-38242	5531

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/711,532	SHARMA ET AL.
	Examiner	Art Unit
	Quan Tra	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-8* is/are allowed.

6)☒ Claim(s) *1-5 and 9-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4, 5, 9 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 is indefinite because the limitation "the drain terminal of said second transistor is connected to said node" is misdescriptive. Claim 3 recites that "said first current source and said second current source drive said node". The drawings does not show that the current source in the primary current block drives the drain terminal of the second NMOS transistor in the backup current block.

Claim 5 is rejected as including the indefiniteness of claim 4.

Claims 9 and 10 are rejected for the same reasons.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Renous (USP 6566935).

As to claim 1, Renous's figure 1 a bias generation circuit for generating a bias current comprising a primary current block (circuit, not shown, that generates V2) generating a primary bias current using a second supply voltage; a backup current block (circuit, not shown, that generates V1) generating a backup bias current; a multiplexor (T1, T2) selecting one of the primary bias current and the backup bias current as the bias current. Thus, figure 1 shows all limitations of the claim except for the backup current block uses a first supply voltage that is higher than the second supply voltage to generate the backup bias current. However, it is notoriously well known in the art that a constant voltage can be generated from a higher voltage by using voltage step down circuit. One skill in the art would have motivated to use a voltage that is higher than V2 to generate V1 if there is no other available voltage source that meet the desired value for V1. Therefore, it would have been obvious to one having ordinary skill in the art to use voltage step down circuit for generating V1 from a supply voltage that is higher than V2 in order to meet the desired value of V1.

As to claim 2, the modified figure 1 shows that the multiplexor selects the backup bias current as the bias current when the second supply voltage is not present (when V2 is lower than V1).

As to claim 3, figure 2 shows that the multiplexor performs the selecting according to a select signal (output of A1) connected to a node, wherein the primary current block comprises a first current source (it is inherent that any voltage generating circuit has current source) and the backup current block comprises a second current source, wherein the first current source and the second current source drive the node.

Claim 11 recite similar limitations of claim 1. Therefore, it is rejected for ther same reasons.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Renous (USP 6566935) in view of Yamauchi (USP 5982162).

The modified Renous' figure 1 shows all limitations of the claim except for the detail of the newly added voltage step down circuit. Yamauchi's figure 3 shows a voltage step down circuit that generates a constant voltage independent of external power supply. Therefore, it would have been obvious to one having ordinary skill in the art to use Yamauchi's voltage step down circuit to generate Renous's V1 for the purpose of improving the circuit performance. Thus, the modified Renous's figure 1 further shows that the second current source comprises: a resistor (Yamauchi's 25) connected between the first supply voltage and a first node; a first NMOS transistor (Yamauchi's 29); and a second NMOS transistor (yamauchi's 31); wherein the drain terminal of the first NMOS transistor is connected to its gate and the first node; the drain terminal of the second NMOS transistor is connected to the node; the gate terminal of the second NMOS transistor is connected to the gate of the first NMOS transistor, and the source of the second NMOS transistor is connected to the source of the first NMOS transistor.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Renous (USP 6566935) in view of Yamauchi (USP 5982162) and Wang (USP 5939933).

The modified Renous' figure 1 shows all limitations of the claim, except for the detail of Yamauchi's current source. However, Wang's figure 4 shows a current source circuit (all elements except for circuit 22) that generates precision current. Therefore, it would have been obvious to one having ordinary skill in the art to use Wang's current source for Yamauchi's

current source for the purpose of generating precision current source. Thus, the modified Renous' figure 1 shows that the backup current source further comprises current mirror circuit.

Allowable Subject Matter

7. Claims 6-8 are allowed.

8. Claims 9 and 10 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 6-8 are and claims 9 and 10 would be allowable because the prior art fails to teach or suggest a device having processor, DAC, filter and line driver, wherein the line driver comprises the current selecting circuit as claimed.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

October 11, 2005